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## **Communication Systems and Protocols**

**Exercise 6** 

## **Controller Area Network (CAN)**





- 1981 developed by Bosch and Intel
- Goal: Cross-linkage of complex controllers and control units
- International dissemination in the automobile area, the sector of home appliance, in textile machines, in medical engineering devices, ...
- Can also be applied as sensor/actuator bus if realtime constraints are kept
- Low priced bus transceivers through high volume number

### **Bus Arbitration**



- Participants are connected to the bus via open collector drivers
  - Dominant LOW, logical ,0'
  - Recessive HIGH, logical ,1'
    - → "Wired-AND"
- Arbitration scheme: CSMA/CA
- Arbitration is done with the help of the identifiers of a message
  - Identifier with the lowest value has got highest priority (dominant ,0').
  - Every identifier can exist only once within the whole system



# Task 1: CAN bus

Time remaining



### **Universal Serial Bus (USB)**



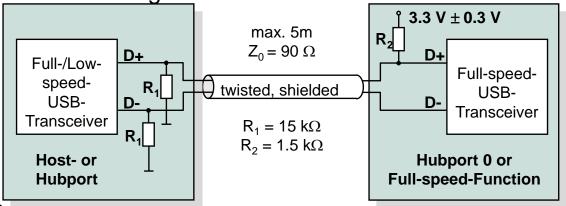


- Serial Bus
- NRZ-I Encoding
- Single Master / Multi Slave
- Hot-Plug Capability

### **Transmission speed detection**



- Devices announce their transmission speed using different pull-up resistors at the data wires
- Example for resistor configuration at 12Mbit/s



- At 1.5Mbit/s<sup>1</sup>
  - Low-Speed Transceiver
  - R<sub>2</sub> at D-
  - Cable does not need to be twisted/shielded
  - Z<sub>0</sub> arbitrary
  - Max. 3m wire length
- High-speed devices announce themselves as Full-speed devices (12Mbit/s) first
  - At configuration time, the host is informed about the higher transmission rate possible
  - In normal operation, the resistor is disabled in order to provide symmetrical wire behavior

### **Energy consumption**



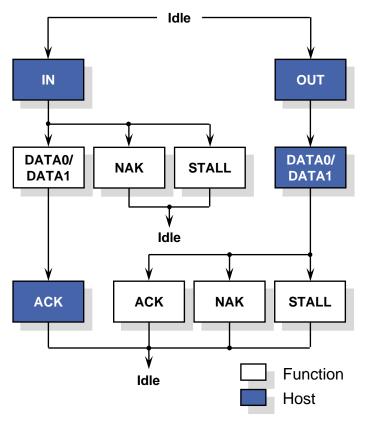
- Devices can be supplied with energy (5V) over the bus
- 3 different classes have to be distinguished
  - Low-power devices: max 100mA
  - High-power devices: max 500mA
  - Self-powered devices: max 100mA from the bus, the rest has to be fetched from their own power supply during operation → otherwise they can be disabled by the host
- Devices have to announce their power consumption at configuration time and are not allowed to go beyond this limit
- Devices have to support standby mode
  - Maximum power consumption of 500μA
  - Devices have to go into standby after 3ms of inactivity on the bus or by dedicated command of the host

### **Transfer process**



- The host starts a transfer by sending a corresponding token packet
- Then one ore more data packets are transmitted
- Each packet is acknowledged by a handshake packet
- If errors have occurred during a transmission, no handshake packet is send. The sender has to retransmit the packet
  - For isochronous transfers there is no handshake. Defective data is not transmitted again!

#### **Exemplary Bulk Transfer:**





# Task 2: Universal Serial Bus (USB)

Time remaining



### **FlexRay**





- Consortium founded in 1999
- Motivation: increasing requirements concerning bandwidth and transmission safety within automobiles
- Goal: Development of deterministic, fault tolerant communication system with 10 MBit/s bandwidth
- Basis for X-by-Wire systems
- Actual specification (Version 2.0) specifies protocol, physical layer and the "Bus Guardian"
- Basically the protocol can be used for optical as well as electrical media.

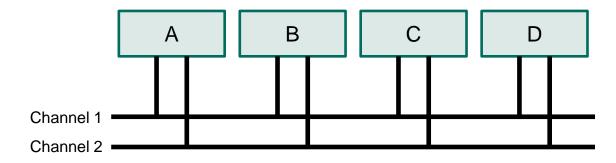
### **Basic features**

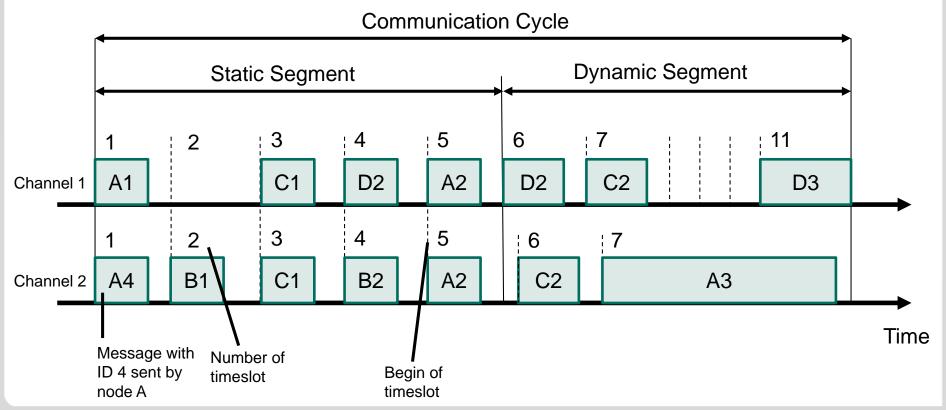


- Multi-master system
- Beside basic star like structure also line and bus structures possible
- Allows operation in channel mode with (10 MBit/s) or double channel mode (20 MBit/s)
  - Single channel mode to increase reliability. The second channel is used as a redundancy.
  - Double channel mode to raise throughput but less reliability
- Mechanisms to increase fault tolerance
  - Deactivation of sub-networks in the case of an error
- Deterministic message transmission by using communication cycles
  - Communication cycle is flexibly configurable
  - Global time base for synchronization
- Physical layer: Differential signalization on a twisted pair
- In contrast to CAN "logic 1" and "logic 0" are equitable



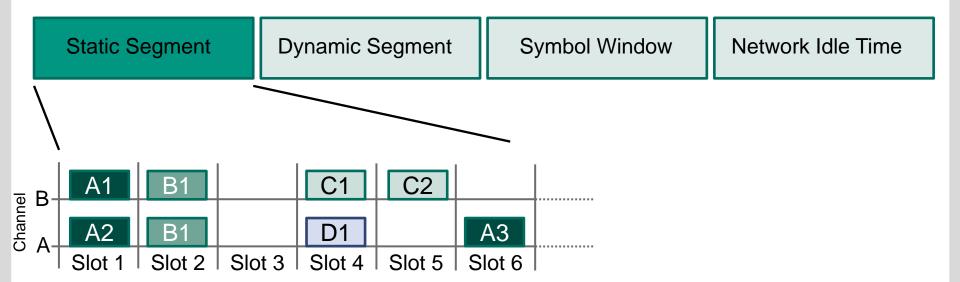
### FlexRay Bus Access





## **Static Segment (1)**

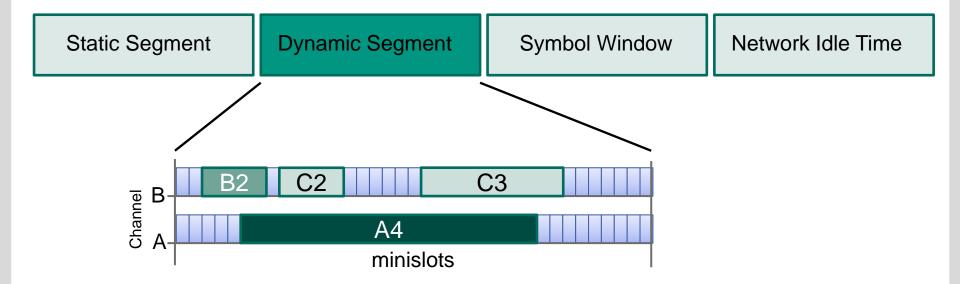




- Nodes are assigned to fix time windows in which frame transmission can be performed
- Bus access within the static segment via TDMA
  - Realization of realtime capability within this segment (deterministic)
  - Every message within this segment is transmitted at defined points in time

### **Dynamic Segment**



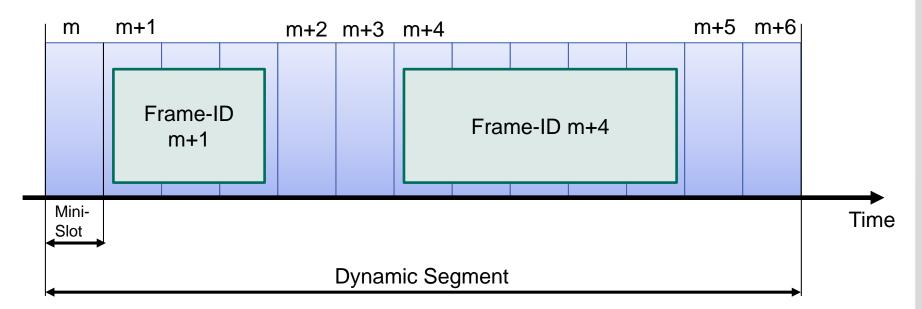


- For frames with lower requirements concerning predictable latency
- Bus access via FTDMA (also called Mini-Slotting)
- Used for event based transmission: Event based data to be transmitted does not depend on a static slot

### **Mini-Slotting (FTDMA)**



- Prioritized bus access within the dynamic segment controlled with a slot count
  - If a Minislot is not used the slot counter is incremented and the Minislot elapses unused
  - If the actual slot count corresponds to the Slot-ID of the frame, the frame occupies a certain number of Minislots. After the next free Minislot the slot counter is immediately incremented
- Space within the dynamic segment can be used efficiently that way





# Task 3: FlexRay

Time remaining

